CLAIMS

1. A method for profiling the frequency that particular ones of a plurality of instructions are executed, said method comprising:

generating an interrupt;

storing an address from a program counter at the time of the interrupt; and

updating a profile with the address from the program counter.

2. The method of claim 1, further comprising:

generating a pseudo-random number after generating the interrupt; and

loading a timer with a value that is a function of the pseudo-random number.

3. The method of claim 2, wherein the value is a function of the pseudo-random number and a user-provided parameter.

4. The method of claim 2, wherein the psuedo-random number is a function of the address from the program counter.

5. The method of claim 1, wherein updating the profile further comprises:

incrementing a count associated with an address range, the address range comprising the address in the program counter.

6. An instruction memory storing a plurality of instructions, said plurality of instructions comprising:

a host operation for performing a host function, the host operation comprising a first plurality of instructions; and

an interrupt subroutine for interrupting the host function, said interrupt subroutine comprising:

a debugging tool for profiling the frequency that particular instructions of the first plurality of instructions are executed.

7. The instruction memory of claim 6, wherein the debugging tool further comprises a second plurality of instructions, said second plurality of instructions further comprising:

updating a profile with the address in the program counter at the time of the interrupt

generating a pseudo-random number after generating the interrupt; and

loading a timer with a value that is a function of the pseudo-random number.

8. The instruction memory of claim 7, wherein the value is a function of the pseudo-random number and a user-provided parameter.

9. The instruction memory of claim 7, wherein the psuedo-random number is a function of the address from the program counter.

10. An integrated circuit for performing a host function, said integrated circuit comprising:

a first memory for storing a host operation comprising a first plurality of instructions,

a processor for executing the first plurality of instructions;

a timer for interrupting the processor; and

a second memory for storing an interrupt subroutine, the processor executing the interrupt subroutine after the timer interrupts the processor; and

the interrupt subroutine comprising:

a debugging tool for measuring the frequency that particular instructions of the plurality of instructions are executed.

11. The integrated circuit of claim 10, further comprising:

a third memory for storing a profile, the profile profiling the frequency that particular instructions of the plurality of instructions are executed.

12. The integrated circuit of claim 10, wherein the debugging tool further comprises a second plurality of instructions, the second plurality of instructions comprising:

updating a profile with the address in the program counter at the time of the interrupt

generating a pseudo-random number after generating the interrupt; and

loading a timer with the pseudo-random number.

13. The integrated circuit of claim 12, wherein updating the profile further comprises:

incrementing a count associated with an address range, the address range comprising the address in the program counter.

14. The integrated circuit of claim 12, wherein the value is a function of the pseudo-random number and a user-provided parameter.

15. The integrated circuit of claim 12, wherein the psuedo-random number is a function of the address from the program counter.